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10/698,532	11/03/2003	Takuya Kobayashi	61282-043	1414

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EXAMINER	
NGUYEN, STEVE N	
ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 05/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/698,532	KOBAYASHI, TAKUYA	
	Examiner	Art Unit	
	Steve Nguyen	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner. for the last line in the Abstract should be deleted.

10)☒ The drawing(s) filed on *16 March 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 8/6/04, 4/22/04, 9/21/05
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-8 are pending and have been examined.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1, 2, 7, and 8 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 1 and 7 recite the limitation, "a clock interval of the time taken for the capturing operation is made variable". However, the time taken for capturing a value into the flip-flop is not dependent upon the clock interval- it is dependent upon the propagation delay of the logic gates of the flip-flop. A signal is captured into a flip-flop by strobing a clock. The signal is captured either on the rising edge or the falling edge of the clock pulse. The clock edge marks the beginning of the time taken for the capturing operation. Therefore it is unclear how a variable clock interval has any relationship to the capturing operation or the time taken for the capturing operation. Furthermore, it is not clear what is meant by "a clock interval of the time taken". The time taken to capture a signal into a flip-flop is significantly shorter than a clock interval to the point that it is negligible. Therefore the "time taken" would not have an

associated clock interval as claimed. Depending claims 2 and 8 are rejected for similar language.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1, 3, 5, and 7 rejected under 35 U.S.C. 103(a) as being unpatentable over Attaway et al (US Pat. 5,701,308; hereinafter referred to as Attaway) in view of Chao et al (US Pat. 6,671,847; hereinafter referred to as Chao).

As per claim 1:

Attaway teaches a path delay measuring circuitry for judging a signal transition time of a combination circuit whose path delay is to be measured, comprising:

- first (Fig. 4, element 18) and a second flip-flop (Fig. 4, element 20) which are connected to an input of the combination circuit (col. 6, lines 31-34) and constitute a scan-chain (col. 6, lines 35-38);
- a third flip-flop which is connected to an output from said combination circuit to constitute the scan chain (col. 6, lines 49-51);
- a pattern creating circuit for creating a test pattern to be set for said first and said second flip-flop (col. 6, lines 17-22);
- a comparison/decision circuit for comparing the output from said third flip-flop and the expected value (col. 6, lines 56-60); and
- a timing signal creating circuit for supplying an operation timing signal to each of the first, second and third flop-flops, said pattern creating circuit and said comparison/decision circuit (col. 10, lines 12-15),
- wherein after a test pattern is set for said first and said second flip-flop by a shifting operation of the scan chain (col. 4, lines 27-31), the output from said combination circuit is taken into said third flip-flop by a capturing operation (col. 9, lines 8-11) and an output from said third flip-flop is compared with an expected value (col. 6, lines 56-60).

Not explicitly disclosed by Attaway is a clock interval of the time taken for the capturing operation is made variable. Chao in an analogous art teaches a pair of variable clock generator circuits for providing a clock signal (col. 6, lines 11-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the variable clock circuit of Chao to provide the test and

system clocks in the clock control circuitry of Attaway shown in Fig. 6. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in order to be able to test timing parameters in the circuit (Chao; col. 2, lines 44-49) and would have recorgnized that varying the clock would have provided a time savings (Attaway; col. 10, lines 27-34).

As per claim 3:

Attaway further teaches a path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops (col. 6, lines 35-38).

As per claim 5:

Attaway further teaches a path delay measuring circuitry according to claim 1, wherein a plurality of flip-flops are provided which are identical to said third flip-flop (col. 6, lines 35-38).

As per claim 7:

Attaway teaches a semiconductor device comprising a plurality of path delay measuring circuits, each path delay measuring circuitry judging a signal transition time of a combination circuit whose path delay is to be measured, said path delay measuring circuitry comprising:

- first (Fig. 4, element 18) and a second flip-flop (Fig. 4, element 20) which are connected to an input of the combination circuit (col. 6, lines 31-34) and constitute a scan-chain (col. 6, lines 35-38);

- a third flip-flop which is connected to an output from said combination circuit to constitute the scan chain (col. 6, lines 49-51);
- a pattern creating circuit for creating a test pattern to be set for said first and said second flip-flop (col. 6, lines 17-22);
- a comparison/decision circuit for comparing the output from said third flip-flop and the expected value (col. 6, lines 56-60); and
- a timing signal creating circuit for supplying an operation timing signal to each of the first, second and third flop-flops, said pattern creating circuit and said comparison/decision circuit (col. 10, lines 12-15),
- wherein after a test pattern is set for said first and said second flip-flop by a shifting operation of the scan chain (col. 4, lines 27-31), the output from said combination circuit is taken into said third flip-flop by a capturing operation (col. 9, lines 8-11) and an output from said third flip-flop is compared with an expected value (col. 6, lines 56-60).

Not explicitly disclosed by Attaway is a clock interval of the time taken for the capturing operation is made variable. Chao in an analogous art teaches a pair of variable clock generator circuits for providing a clock signal (col. 6, lines 11-16). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use the variable clock circuit of Chao to provide the test and system clocks in the clock control circuitry of Attaway shown in Fig. 6. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have been motivated to do so in

order to be able to test timing parameters in the circuit (Chao; col. 2, lines 44-49) and would have recorgnized that varying the clock would have provided a time savings (Attaway; col. 10, lines 27-34).

4. Claims 2, 4, 6, and 8 rejected under 35 U.S.C. 103(a) as being unpatentable over Attaway in view of Chao in view of Lee et al (US Pat. 6,040,725; hereinafter referred to as Lee).

As per claim 2:

Attaway and Chao further teach a path delay measuring circuitry according to claim 1, further comprising:

- a clock mode counter for outputting a clock mode value which is updated whenever said signal transition time is decided (Attaway, col. 10, lines 22-27; a clock mode value RUN_TEST is provided by the TAP control device); and
- a clock creating circuit for creating another clock to be supplied to said path delay measuring circuit on the basis of said high speed clock and said clock mode value (Chao, Fig. 5; elements 210 and 212 supply the clocks based on the clock mode value provided as disclosed by Attaway above),
- wherein the clock created by said clock creating circuit is made variable in its clock interval of the time to be taken for said capturing operation according to said clock mode value (Attaway; col. 10, lines 22-27).

Not explicitly disclosed by Attaway or Chao is a multiplying circuit for creating a high speed clock on the basis of a clock externally supplied. However, Lee in an analogous

art teaches a clock multiplier circuit for creating a high speed clock (Fig. 1, element 12). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a clock multiplier in the combined system of Attaway and Chao. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that clock multipliers for creating high speed clocks are well known in the art (col. 5, lines 52-53).

As per claim 4:

Attaway further teaches a path delay measuring circuitry according to claim 2, wherein a plurality of flip-flops are provided which are identical to said first and second flip-flops (col. 6, lines 35-38).

As per claim 6:

Attaway further teaches a path delay measuring circuitry according claim 2, wherein a plurality of flip-flops are provided which are identical to said third flip-flop (col. 6, lines 35-38).

As per claim 8:

Attaway and Chao further teach a semiconductor device comprising as claimed in claim 7, wherein said path delay measuring circuitry further comprises:

- a clock mode counter for outputting a clock mode value which is updated whenever said signal transition time is decided (Attaway, col. 10, lines 22-27; a clock mode value RUN_TEST is provided by the TAP control device); and

- a clock creating circuit for creating another clock to be supplied to said path delay measuring circuit on the basis of said high speed clock and said clock mode value (Chao, Fig. 5; elements 210 and 212 supply the clocks based on the clock mode value provided as disclosed by Attaway above),
- wherein the clock created by said clock creating circuit is made variable in its clock interval of the time to be taken for said capturing operation according to said clock mode value (Attaway; col. 10, lines 22-27).

Not explicitly disclosed by Attaway or Chao is a multiplying circuit for creating a high speed clock on the basis of a clock externally supplied. However, Lee in an analogous art teaches a clock multiplier circuit for creating a high speed clock (Fig. 1, element 12). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to use a clock multiplier in the combined system of Attaway and Chao. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that clock multipliers for creating high speed clocks are well known in the art (col. 5, lines 52-53).

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steve Nguyen whose telephone number is (571) 272-7214. The examiner can normally be reached on M-F, 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Steve Nguyen
Examiner
Art Unit 2138

GUY LAMARRE
PRIMARY EXAMINER